REMARKS

Claims 1 - 19 remain active in this application. Claims 1 - 9 have been withdrawn from consideration as being non-elected, with traverse, in response to a requirement for restriction. The indication of allowability of claims 13 - 15 is again noted with appreciation. Amendment of the specification has been requested in response to a criticism by the Examiner. Amendment of claims 10, 13 - 15 and 17 - 19 has been requested to improve form and descriptiveness in response to criticisms by the Examiner. No new matter has been introduced into the application.

The Examiner has adhered to the requirement for restriction and made the requirement final. However, the traverse of the requirement presented in the previous response is respectfully maintained. It is again respectfully submitted that, in describing a materially different method, has not shown that the structure resulting from such a materially different method would be the same as that claimed and thus has not demonstrated that the inventions identified by the Examiner are distinct. The Examiner has not addressed this issue in the impropriety of the requirement in the present office action. Therefore, it is respectfully requested that a proper requirement for restriction be stated on the record or the requirement withdrawn.

The Examiner has objected to the specification as containing an incorrect reference numeral. This objection is respectfully traversed as moot in view of the amendment requested above which corresponds to drawing corrections previously submitted and found acceptable. Accordingly, reconsideration and withdrawal of this objection are respectfully requested.

Claims 13 - 19 have been rejected under 35 U.S.C. §112, second paragraph, due to inadequate antecedent

language correspondence. This ground of rejection is respectfully traversed as being moot in view of the above-requested amendments which adopt the Examiner's suggestions. Accordingly, reconsideration and withdrawal of this ground of rejection are respectfully requested.

Claims 10 - 12 and 16 - 19 have again been rejected under 35 U.S.C. §102 as being anticipated by Hachimene et al. This ground of rejection is again respectfully traversed for the reasons of record and the further reasons detailed in the following remarks.

It was previously pointed out that Hachimene et al. does not attribute the recited function of "shear force isolation" to layer 15 at any mention of layer 15 in the text thereof. In the present action, the Examiner relies only on the text of paragraph 170 of Hachimene et al. which describes layer 15 only as "an insulating film 15 made of, for example, a silicon oxide film" (which is used as an etch stop material for later removal of layer 14b, as previously pointed out) while the Examiner asserts layer 15 to be a "shear force isolation layer". Since Hachimene et al. does not similarly refer to that property or function of layer 15 but, on the contrary, discloses removal of layer 14b to complete the product and, moreover, discusses adverse effects if layer 14b is not removed (at paragraph 0214, as previously pointed out), clearly indicating that no shear stress isolation is obtained therefrom, it appears that the Examiner, without so stating, is applying an inherency rationale in support of this ground of rejection.

For anticipation to be shown, as the Examiner is aware, every recitation of the claim must be answered by a evidence contained in a single document, either explicitly or through inherency. For a rationale of anticipation by inherency, the recited subject matter which is not directly disclosed in the document relied

upon must necessarily and unavoidably flow from subject matter which is, in fact, disclosed in the document relied upon. While the shear stress isolation layer 12, 120 of the present invention is also a dielectric oxide layer (formed, however, by high density plasma deposition as noted at page 11, lines 10 - 25), not all dielectric layers and not even all silicon oxide layers can provide stress isolation. Further, any (incorrect) inference that dielectric layers are necessarily capable of providing shear stress isolation would be an exercise in speculative hindsight through an overbroad interpretation of the present disclosure and not an inherent feature necessarily and unavoidably flowing from subject matter actually disclosed by Hachimene et al., particularly in view of the description of the stress interaction with stressed layer 14a if stressed layer 14b is not removed where it overlies layer 14a, *even if layer 15 were to be left in place*, thus clearly indicating that Hachimene et al. did not achieve or observe stress isolation from the exemplary silicon oxide insulating film disclosed for layer 15 but, on the contrary, that Hachimene et al. observed that stress isolation was not, in fact, achieved.

More specifically, and even in regard to only silicon oxide materials mentioned by Hachimene et al., it is respectfully brought to the Examiner's attention that it is well-known in the art that stresses can be carried by silicon oxide and/or to use silicon oxide to *impart* stress to semiconductor structures rather than to *isolate* structures from it. In addition to the clear indication that Hachimene et al. does not observe or achieve stress isolation with silicon oxide layer 15 (and, hence, does not provide evidence that a "stress isolation layer" between stressed layers was known or used by others prior to the invention by Applicants), exemplary of such observations of imparting or communicating stress through silicon oxide are "Novel

Locally Strained Channel Technique for High Performance 55nm CMOS" by Ota et al. (IEEE, 2002) and "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress" by Scott et al. (IEEE, 1999), copies of which are attached. These articles clear describe the imparting or communicating of stress through silicon oxide. Therefore, since stress isolation does not *necessarily and unavoidably flow* from the disclosure of silicon oxide in Hachimene et al., particularly in view of the disclosure at paragraph 0214 of Hachimene et al. clearly and strongly indicating that stress isolation was not observed in layer 15, and the attached articles, it is respectfully submitted that the Examiner has not made a proper and *prima facie* demonstration of anticipation through inherency but has assumed a property (and function) not mentioned by Hachimene et al. (contrary to the clear implications of paragraph 0214 thereof) through speculative hindsight based on an improper interpretation of the present disclosure.

Accordingly, it is respectfully submitted that the sole ground of rejection asserted in this application is clearly in error and is untenable. Therefore, it is respectfully requested that the ground of rejection based on Hachimene et al. be reconsidered and withdrawn.

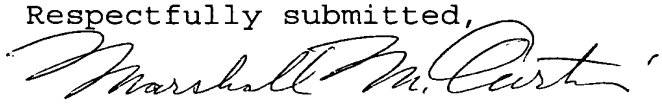
Additionally, it is respectfully submitted that entry of the above-requested amendments is well - justified. No new issue is or can be raised thereby since the amendments are limited to direct responses to the Examiner's criticisms in regard to matters of form; entry of which is explicitly provided for in 37 C.F.R. §1.116. Moreover, entry is well-justified as placing the application in condition for allowance or, in the alternative, better form for Appeal by materially reducing and simplifying issues. Additionally, the finality of the present action is respectfully

submitted to be premature and should be withdrawn since the Examiner continues to fail to make a proper requirement for restriction or other answer to the traverse made. Accordingly, entry of the above-requested amendments is respectfully submitted to be in order.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0458 of International Business Machines Corporation (East Fishkill).

Respectfully submitted,



Marshall M. Curtis
Reg. No. 33,138

Whitham, Curtis & Christofferson, P. C.
11491 Sunset Hills Road, Suite 340
Reston, Virginia 20190

(703) 787-9400
Customer Number: **30743**

NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress

Gregory Scott, Jeffrey Lutze, Mark Rubin, Faran Nouri, and Martin Manley

Technology Development, Philips Semiconductors
1109 McKay Drive, San Jose, CA 95131

Abstract

This paper describes a previously unreported phenomenon wherein NMOS transistors of identical gate length exhibit a significant sensitivity to layout. Drive current may be reduced up to 13%, depending on diffusion overlap of gate. Mobility reduction, induced by stress from the trench isolation edge, is the root cause of the performance degradation. PMOS devices are not affected. Simulation results show that stress varies strongly with distance from the trench edge, and with overall diffusion size. Stress is also a major component of narrow-width effects, and explains why Idsat scaling with W differs for NMOS and PMOS devices.

Introduction

As CMOS devices continue to be scaled, effects that had once been considered secondary are becoming more important. The details of device layout, particularly the diffusion overlap of gate, have a significant effect on transistor performance. NMOS test devices drawn with relatively loose design rules may behave quite differently from transistors in an actual product, even when physical gate dimensions are the same.

Stress from the trench isolation edge is the dominant factor affecting layout sensitivity. Previous studies have shown that stress can affect device workfunction and bandgap (1), carrier mobility (2-7), junction leakage (8), and hot-electron lifetime (9). Simulation results show that trench-induced stress is of the order needed to produce the observed degradation in device performance.

Transistor Data

Transistors produced with a 0.2 μm process internally and a different process at a foundry site displayed noticeable sensitivity to transistor layout. As the diffusion size in the gate-length direction (L') was reduced to below 2 μm, Idsat dropped (Fig. 1) by 5-10%. A variety of test structures were developed to study layout sensitivity in more detail (Fig. 2): 0.2 μm transistors with small, medium and wide overlap, and wide overlap with asymmetrical gate placement. Medium-overlap transistors with different gate lengths were also included. Top-down and cross-sectional measurements confirmed that the poly dimensions of all 0.2 μm devices

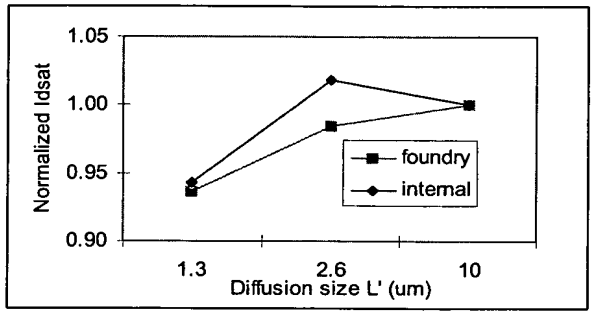


Fig. 1 Idsat vs. diffusion size in gate-length direction L' (see Fig. 2) for foundry and internal 0.2um NMOS devices. Idsat is normalized to 1 for the L'=10um device.

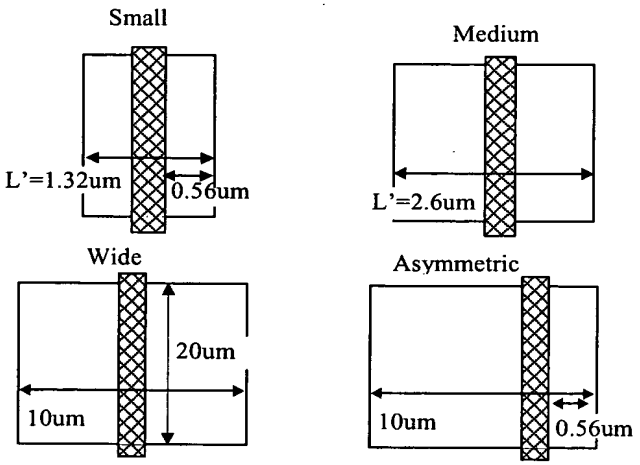
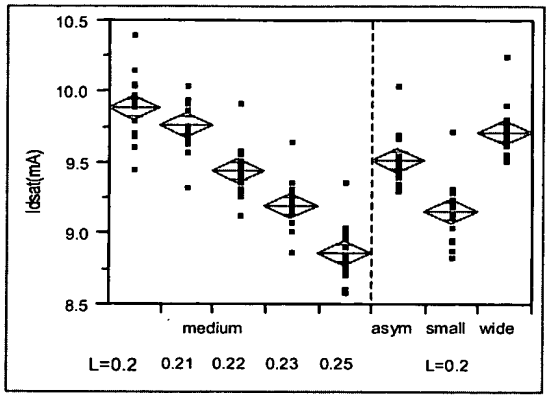


Fig 2. Layout of 0.2μm gate length transistors used in this study. All transistors were 20μm wide.

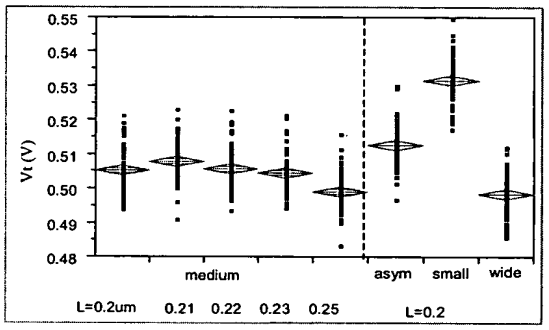
varied by less than 10 nm..

Mean Idsat of a 0.2 μm device was reduced by 7% as L' was reduced from medium to small layout, while asymmetric layout gave a reduction of 4% (Fig. 3a). The reduction in drive current seen with the small overlap corresponds to an increase in gate length of 30 nm; this is clearly a significant change. The small overlap devices also had a 25 mV increase

0-7803-5413-3/99/$10.00 (c) 1999 IEEE



(a)



(b)

Fig 3. NMOS Idsat and Vt vs. device layout. The degradation in Idsat of a small overlap 0.2um transistor is equivalent to a 30 nm increase in gate length.

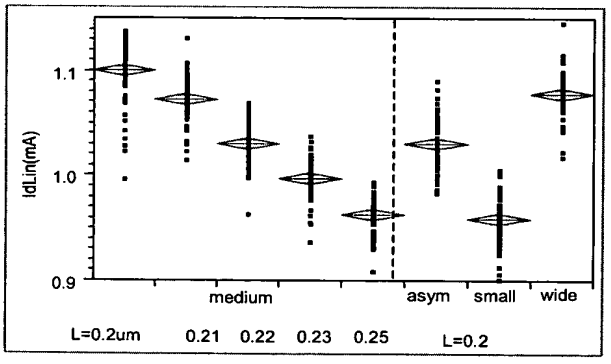
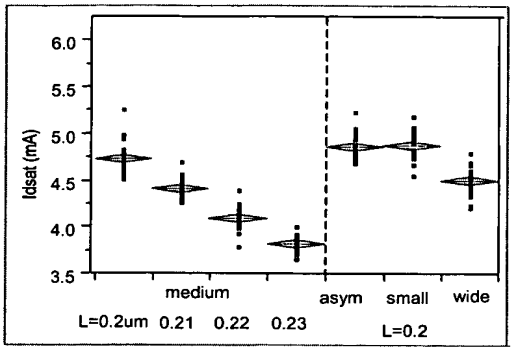
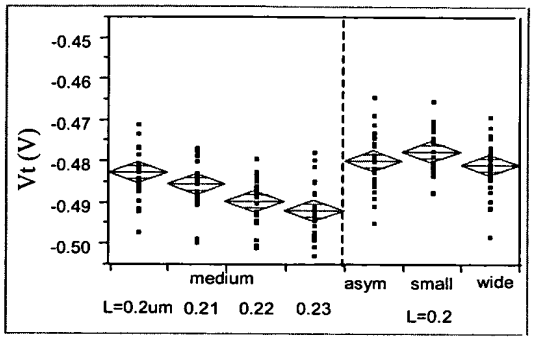


Fig. 4. Linear Id (Vg=1.8, Vd=0.05V) for different device layouts. The degradation in Id linear of a small overlap transistor is equivalent to a 50 nm increase in gate length.



(a)



(b)

Fig 5. PMOS Idsat and Vt layout dependence.

in Vt over the medium overlap device (Fig. 3b), but this Vt offset only accounts for a 2% reduction in Idsat. Linear Id (Vg=1.8, Vds=0.05V) was even more sensitive then Idsat, showing a 13% reduction as L' was reduced from medium to small overlap (Fig. 4), indicating that series resistance is not the cause of the drive current reduction. Moreover, the asymmetric device gave the same current when source and drain were reversed, arguing against an effect from silicide interfacial resistance. Proximity of the gate to the trench edge and overall diffusion size appeared to be the most significant factors. In contrast, PMOS devices exhibit little sensitivity to layout (Figs. 5a and 5b).

While the devices with various layouts had the same physical gate length, it was possible that L_{eff} differences were leading to the drive current variation. However, since L_{eff} extraction algorithms assume that mobility remains constant with varying L, we could not rely on them for this analysis. Instead, we used DIBL as a measure of the electrical channel length. DIBL measurements (Fig. 6) show that a 30nm increase in L_{eff}, which would be necessary to create the

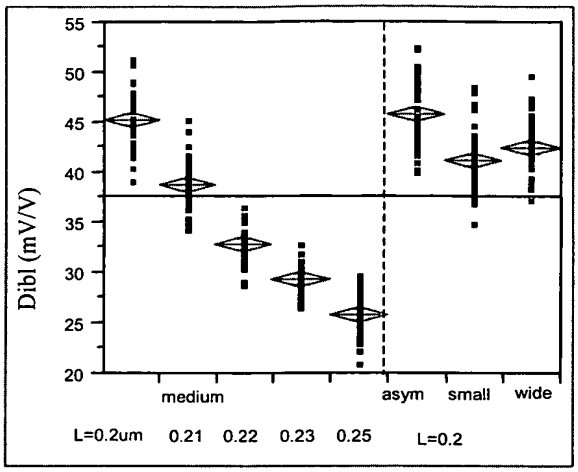


Fig 6. DIBL vs. layout type for NMOS devices. There is little difference in DIBL between 0.2um layouts, as opposed to Idsat.

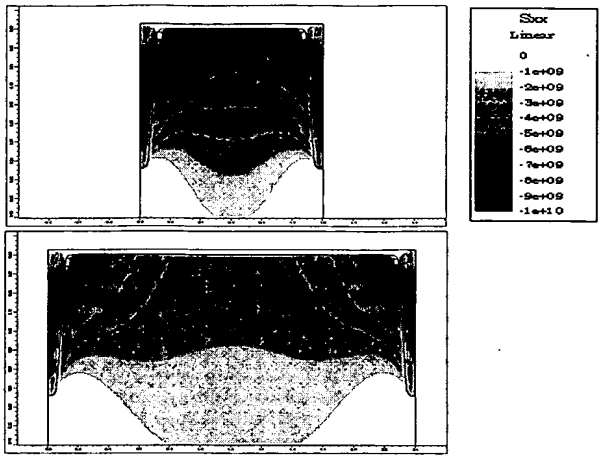


Fig 8. Stress simulation of small and medium overlap transistors

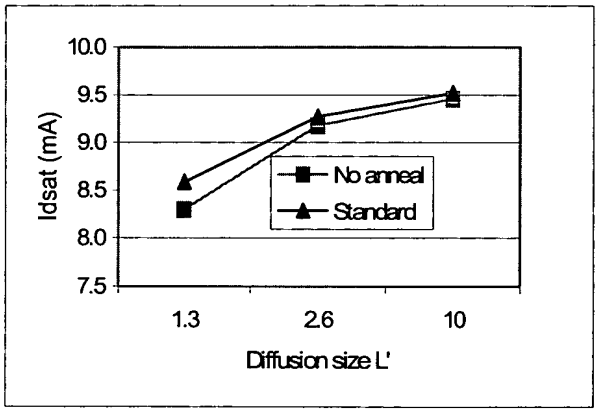


Fig. 7. Effect of no post-trench anneal on 0.2um NMOS Idsat reduction

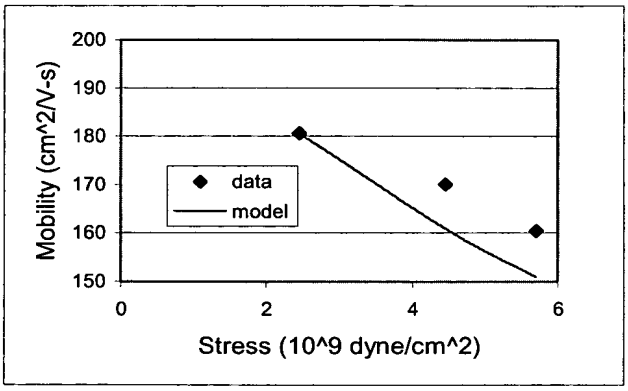


Fig. 9. Mobility dependence on simulated stress

observed reduction in drive current, would produce a 16mV/V drop in DIBL, while the DIBL offset between small and medium overlap devices was less than 4mV/V. This indicates that L_{eff} is essentially the same for all transistor layouts.

The only reasonable explanation for the drive current reduction is mobility degradation. Literature data indicates that compressive stress in silicon, through the piezoresistive effect, causes a reduction in electron mobility, while it has a minimal effect on hole mobility (3,4). Therefore, NMOS devices will be affected more by trench stress than PMOS, as we have observed. To further verify this model, wafers were processed without a post-trench-anneal step, which is known to increase stress in the silicon. As expected, NMOS devices processed without the anneal showed even greater sensitivity to the transistor layout (Fig. 7).

The change in Vt between large and small overlap devices was greater for high-Vt transistors, which have more boron in the channel. This indicates that stress-enhanced diffusion (10) is one factor contributing to the Vt offset.

Simulation Results

SUPREM simulations show that stress in the diffusion area varies strongly with the size of the diffusion, increasing from 2.4 to 5.7×10^9 dyne/cm^2 as L' shrinks from 2.4 to 1.2um (Fig. 8). Further simulations show that the asymmetric layout creates a stress of 4.7×10^9 dyne/cm^2 under the gate. Plotting

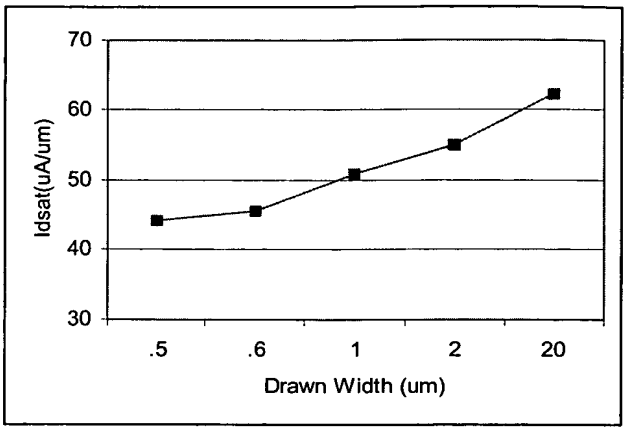


Fig. 10. Idsat (μA/μm) of L=2μm NMOS devices of various widths. The gate overdrive (V_g-V_t) was normalized to eliminate the impact of Vt rolloff.

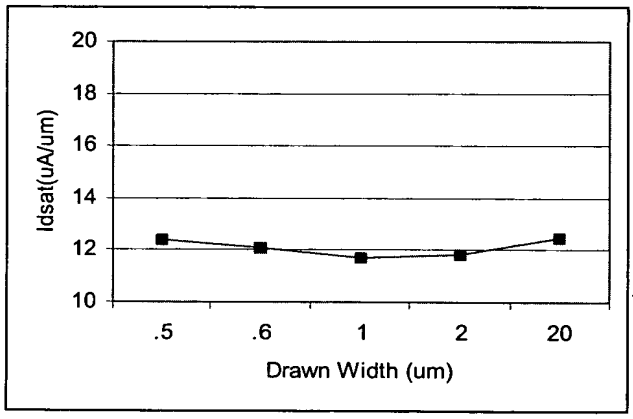


Fig. 11. Idsat (μA/μm) of L=2μm PMOS devices of various widths. The gate overdrive (V_g-V_t) was normalized to eliminate the impact of Vt rolloff.

electron mobility extracted from linear current measurements as a function of simulated stress (Fig. 9), we observe qualitative agreement with simple calculations based on the piezoresistance model.

Narrow Devices

Narrow NMOS devices also exhibit Idsat reduction as the width is decreased. Fig. 10 is a plot of Idsat vs. device width for L=2μm transistors. We chose longer channel devices to avoid complications of short-channel effects and velocity saturation. Reduction in Idsat is normally modeled by an effective-width decrease. However, there is essentially no trench encroachment in this case. Moreover, PMOS devices are not affected over this range of W (Fig. 11). The same stress-dependent mobility phenomenon described above appears to be operating here. The highly stressed region near the trench edge becomes a greater fraction of the total device width as W decreases; stress in the center of the active region increases at the same time.

Summary

We have shown that mobility reduction due to stress from trench isolation makes NMOS drive current highly sensitive to transistor layout. Trench stress is also a major component of narrow-width effects, and helps to explain why NMOS and PMOS devices behave differently as W is scaled. These effects will increase as design rules are shrunk for future generations.

References

(1) H. Rueda, J. Slinkman, D. Chidambarrao, L. Moszkowicz, P. Kaszuba, M. Law, *Mat. Res. Soc. Symp. Proc.* 568, p. 245, 1999

(2) J.L. Egley, D. Chidambarrao, *Sol. St. Electron.* 36, p. 1653 (1993)

(3) J. Hynecek, *J. Appl. Phys.* 45, p.2631 (1974)

(4) B-Y Tsaur, J. Fan, M.W. Geis, *Appl. Phys. Lett.* 40, 322 (1982)

(5) A. Hamada, T. Furusawa, N. Saito, E. Takeda, *IEEE Trans. Electron Devices* ED-38, p. 895 (1991)

(6) J. Wesler, J.L. Hoyt, S. Takagi, J.F. Gibbons, *IEDM Tech Digest*, p. 373, 1994

(7) J. E. Dijkstra, W. Th. Wenckebach, *J. Appl. Phys.* 81, p.1259 (1997)

(8) P. Smeys, P. B. Griffin, Z. U. Rek, I. De Wolf, K. Saraswat, , *IEEE Trans. Electron Devices* ED-46, p. 1245 (1999)

(9) B. Borchert, G. E. Dorda, *IEEE Trans. Electron Devices* ED-35, p. 483 (1988)

(10) P. Kuo, J.L. Hoyt, J.F. Gibbons, J.E. Turner, and D. Lefforge, *Appl. Phys. Lett.* 66, 580 (1995)

0-7803-5413-3/99/$10.00 (c) 1999 IEEE

Novel Locally Strained Channel Technique for High Performance 55nm CMOS

K. Ota, K. Sugihara, H. Sayama, T. Uchida, H. Oda, T. Eimori, H. Morimoto and Y. Inoue
ULSI Development Center, Mitsubishi Electric Corporation
4-1 Mizuhara, Itami, Hyogo 664-8641, Japan
Tel.:+81-727-84-7322 Fax:+81-727-80-2675 e-mail: kaohta@lsi.melco.co.jp

Abstruct

A novel local strained channel (LSC) MOSFET has been fabricated by a stress control technique utilizing a strained poly silicon gate electrode. The residual compressive stress in arsenic (As) implanted poly silicon is induced by high temperature annealing of CVD SiO_2 cap with high tensile stress. On the other hand, boron (B) implanted poly silicon is free from stress. As a result, the only n-channel region is locally strained by the strained poly silicon electrode. The drain current of LSC nFETs is improved 15% compared to that of the conventional nFET without the degradation of pFET drain current. High performance 55nm CMOSFET is realized by simple process for LSC-structure.

Introduction

As an ultimate solution of CMOSFET scaling limits, the improvement of electron and hole mobility has been extensively studied by introducing strain in channel region [1-3]. Strained silicon devices on SiGe substrate have been proposed which uses Si/SiGe lattice mismatch, since the biaxial tensile strain improves both electron and hole mobility. However, this kind of strained silicon devices has many difficulties in manufacturing. On the other hand, local mechanical-stress controlled (LMC) MOSFETs' have been proposed, which form uniaxially-strained channel by utilizing a contanct etch-stop silicon nitride layer as a stressor [4-6]. However, uniaxial tensile strain degrades the hole mobility, while compressive strain degrades the electron mobility [7]. In order not to degrade either of them, LMC technique needs additional Ge implantation to remove the strain [6]. In this study, a novel locally strained channel (LSC) technique is proposed which provides tensilely-strained channel only in nFET by forming compressively strained polycrystalline Si (poly-Si) gate electrodes. Compressive stress of N-gate, which is enhanced by cap-annealing process, derives from expansion of As-implanted poly-Si. On the other hand, p-channel is not strained, because B-implanted poly-Si is hardly expanded. We experimentally demonstrate the improvement of drivability of nFETs without degrading the drivability of pFETs. Finally, we show high performance 55nm CMOSFET.

Experimental

The fabrication process of LSC MOSFET is illustrated in Fig. 1. After implantations for source/drain regions, CVD

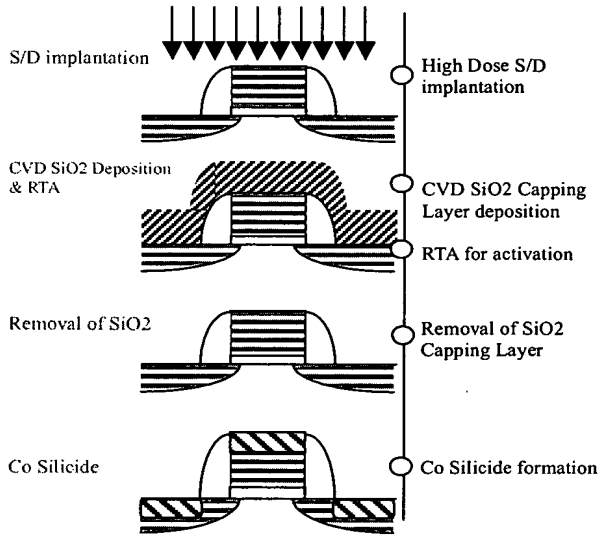


Fig. 1 Fabrication process for locally strained channel (LSC) transistor.

SiO_2 layer was deposited. The temperature of deposition should be lower than the phase transition temperature of amorphous silicon. Then, rapid thermal annealing was carried out at high temperature. After the CVD SiO_2 layer was removed, a Co silicide film was formed according to the conventional Co salicide process.

Results and discussions

The cross-sectional SEM images of as-etched gate electrodes of nFET and pFET are shown in Figs.2 (a) and (b), respectively. Those gate electrodes have flat sidewall shape. There is no difference between nFET and pFET. However, Figs. 2 (c) and (d) show the significant difference between full-processed LSC-nFET and pFET. Although the shape of P-gate hardly changes after full process, N-gate shows the deformed shape, where the upper half of N-gate seems to be compressed. Thus, N-gate has residual stress, while P-gate is free from stress. The detailed mechanism of N-gate residual stress generation is as follows; before the activation annealing process, the upper half of N-gate is in amorphous phase due to the high dose implantation of arsenic. The re-crystallization of amorphous region during the annealing process leads to N-gate expansion and residual compressive stress. Furthermore, CVD SiO_2 cap-annealing enhances compressive strain in N-gate, since CVD SiO_2 is highly tensile. Therefore, the strain in N-gate provides high

0-7803-7463-X/02/$17.00 (C) 2002 IEEE

tensile stress to the channel region.

The stress distributions are simulated as shown in Figs. 2 (e), (f) and (g). Simulation studies are carried out on an assumption that N-gate has uniform stress and P-gate has no stress. For simplicity, poly-Si gate electrode is assumed to retain the capping layer stress. Figures 2 (e) and (f) show the stress distribution of nFET and pFET with CVD SiO_2 cap-annealing. The results show that the channel stress is controlled by strained poly-Si gate electrode. Figure 2 (g) shows the nFET stress distribution without capping layer. It is clearly shown that the channel stress depends upon the capping layer thickness.

Figure 3 shows Ion-Ioff characteristics of CMOSFET with and without the LSC-process. The drain current of short-channel LSC-nFETs is 15% improved compared to that of the conventional nFETs, where capping layer has been removed after the annealing. The improvement of nFET drain current (I_{dn}) is in proportion to capping layer thickness as shown in Fig.4. The transconductance ($g_{m\,max}$) of nFET increases with an increase in capping layer thickness as shown in Fig.5. This fact means that the increase of carrier mobility is the cause of the observed enhancement of drain current. The simulated channel stress dependence on capping layer exhibits the same tendency, as shown in Fig. 6. Figure 7 shows C-V characteristics of LSC and conventional nFET. The inversion capacitance of LSC-nFET is almost the same as that of conventional nFET. Therefore, the increase of I_{dn} is not due to the suppression of poly depletion effect by cap-annealing process but due to the channel stress applied by strained poly-Si electrode. On the other hand, the drain current of pFET is not influenced by LSC process, because P-gate has no residual strain.

The improvement of I_{dn} by LSC process also depends upon the gate length as shown in Fig. 8. The improvement of I_{dn} is more pronounced for short channel device. This improvement is also explained by channel stress simulation (Fig. 9). Averaged stress over the channel region in long channel transistor is smaller than that in short channel transistor, as shown in Fig. 10. As a result, LSC-process is very effective for sub-100nm short channel FETs.

By LSC technique, we fabricated 55nm high performance CMOSFET with 1.7nm physical oxide thickness of gate dielectric. The drain currents at Vcc=1.0V are 800 μA/μm for nFET and 300 μA/μm for pFET at off-current of 20 nA/μm as shown in Fig. 13.

Conclusion

LSC-process that modulates the channel stress by using the stress of poly-Si gate is proposed. The drain current of nFET is improved 15% and that of pFET is preserved. The fabrication of 55nm CMOSFET with high drain current is realized by simple process for LSC-structure.

References

1. J. J. Welser, et al., IEDM Tech. Dig., p1000, 1992
2. C. K. Maiti, et al., Semicond. Sci. Technol., vol. 13, p1225, 1998
3. T. Mizuno, et al., IEEE Trans. Elec. Devices, Vol. 48, p.1612, 2001.
4. F. Ootsuka et al., IEDM Tech. Dig., p.575, 2000.
5. S. Ito et al., IEDM Tech. Dig., p.247, 2000.
6. A. Shimizu et al. IEDM Tech. Dig., p433, 2001.
7. H. S. Momose et al., IEDM Tech. Dig., p.65, 1990.

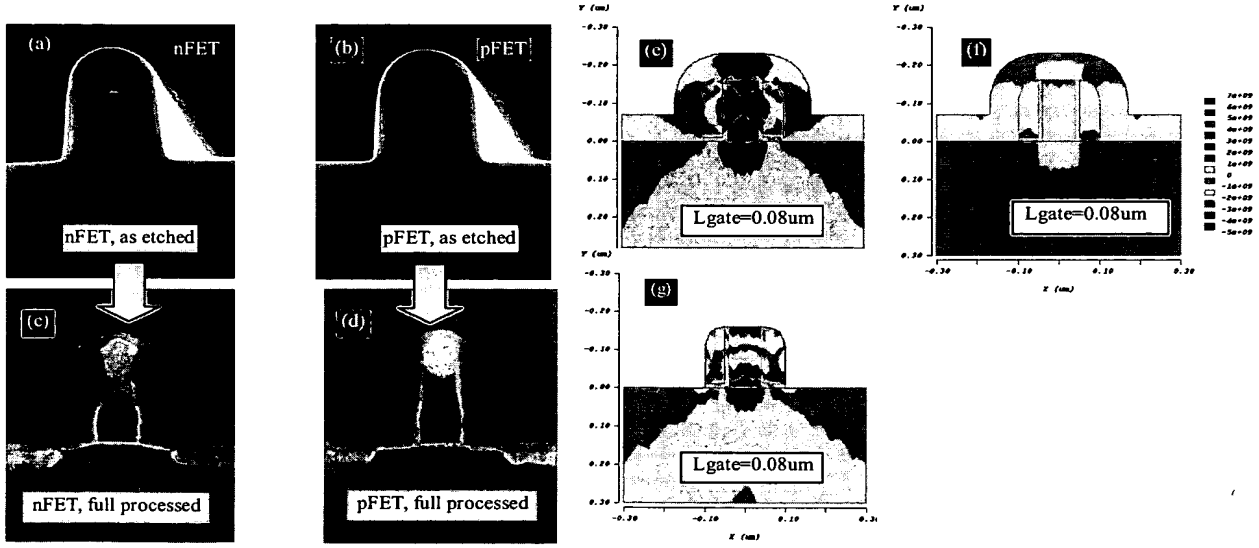
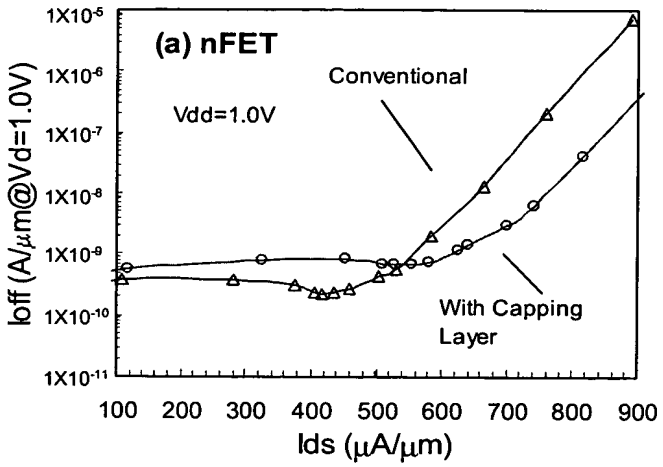


Fig. 2 The cross sectional SEM images and stress distributions of nFET and pFET. (a) as-etched gate electrode of nFET, (b) as-etched, pFET, (c) full-processed gate electrode of nFET, (d) full-processed, pFET.
The simulated stress distributions are shown in (e)nFET with capping layer, (f)pFET with capping layer, (g)nFET without capping layer.



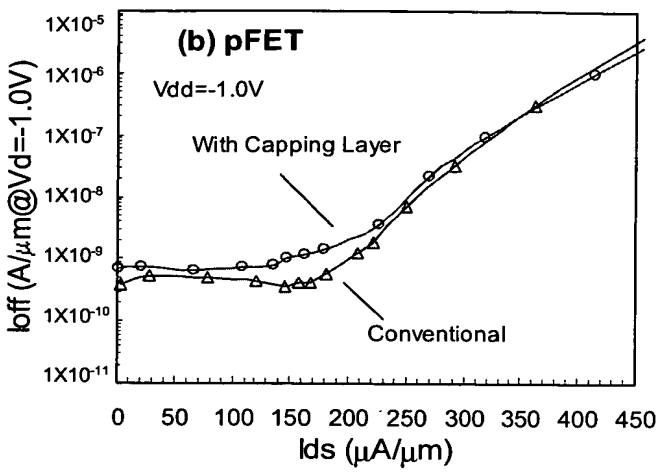


Fig. 3 Ion-Ioff characteristics of (a) nFET and (b) pFET. The drain current of nFET is improved by annealing with capping layer while that of pFET is almost the same.

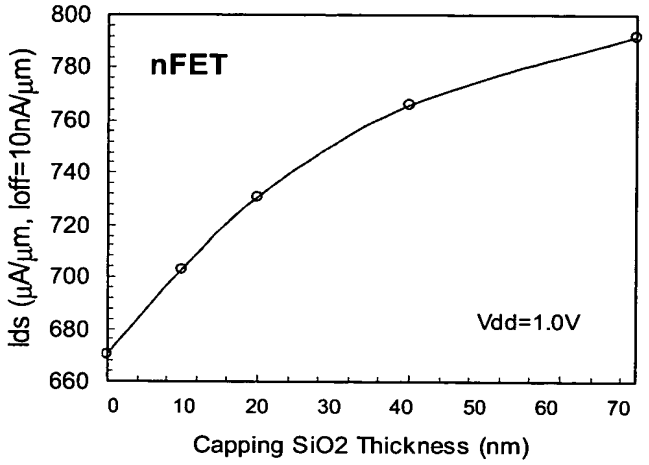


Fig. 4 The dependence of Idn on capping SiO2 layer thickness.

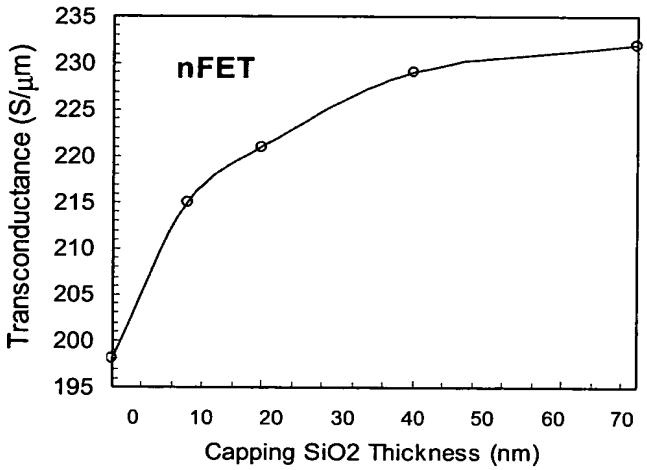


Fig. 5 The dependence of maximum transconductance (gm max) on capping SiO2 layer. Gm max represents carrier mobility because the effective channel length extracted by overlap capacitance is constant.

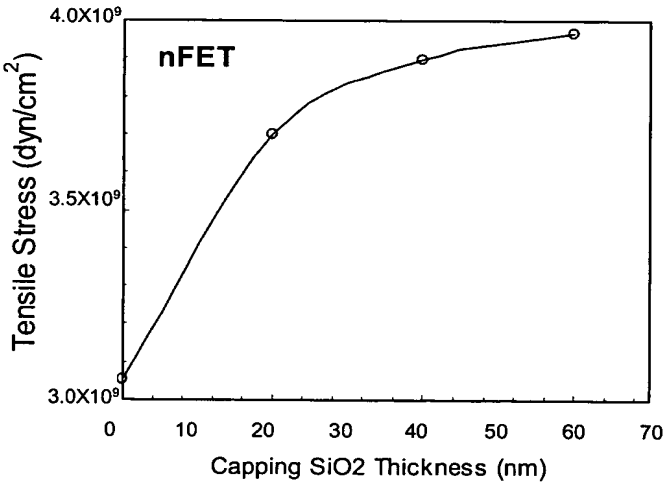


Fig. 6 The dependence of simulated tensile stress at the center of the channel of 0.08um nFET on CVD-SiO2 thickness. Tendencies are similar to Fig. 5.

0-7803-7463-X/02/$17.00 (C) 2002 IEEE

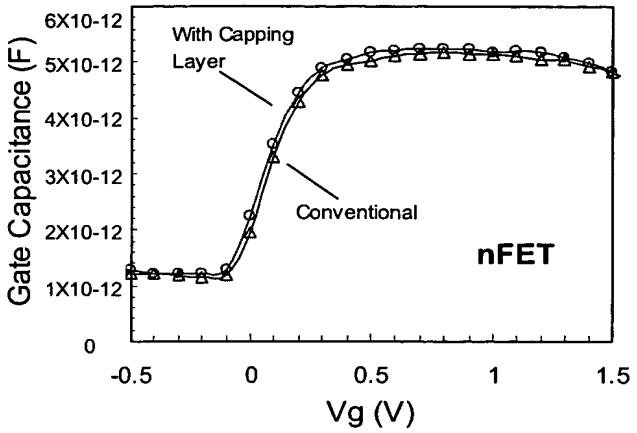


Fig. 7 CV characteristics of nFET with and without capping SiO2 layer. The inversion capacitance with capping layer is almost the same as that without capping layer.

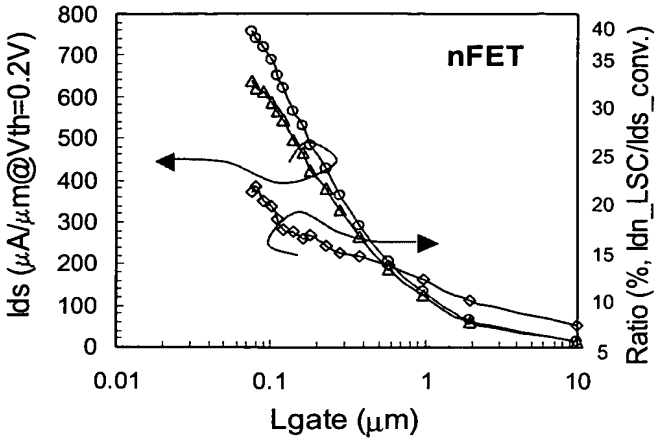


Fig. 8 The dependence of Idn on Lgate are plotted to the left axis. The ratio (Idn_LSC/Idn_conventional) is plotted to the right axis. The ratio strongly depends on the gate length.

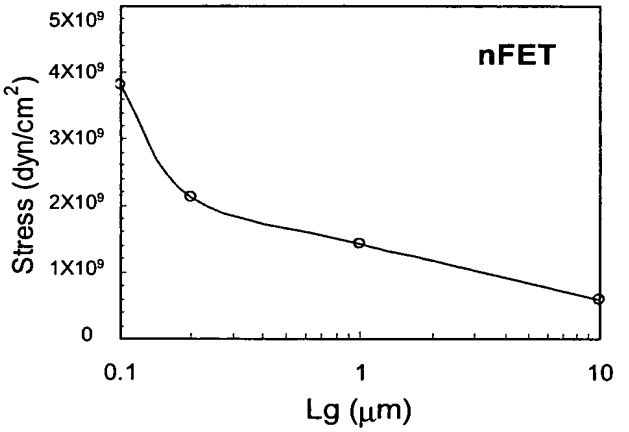


Fig. 9 Simulated n-channel averaged stress over channel region as a function of gate length.

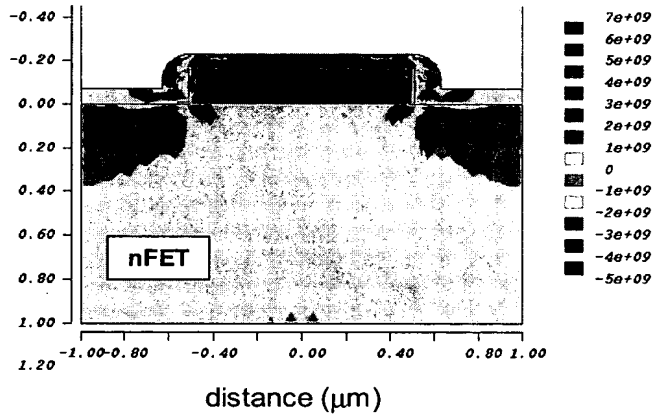
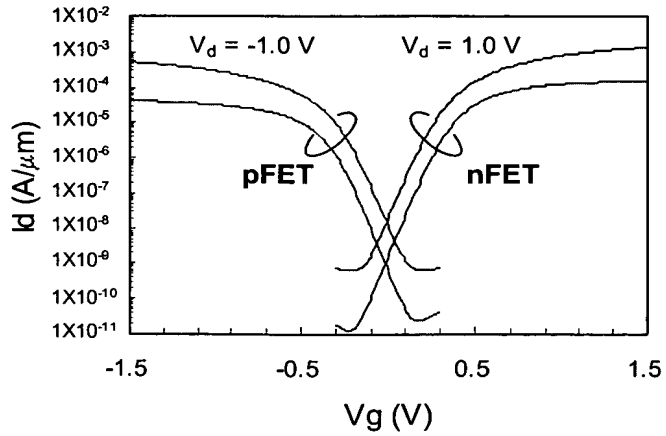


Fig. 10 2Dimensional smilated stress distribution for long channel LSC-nFET. Averaged stress over the channel region in long channel transistor is smaller than that in short channel transistor (Fig. 2(e))



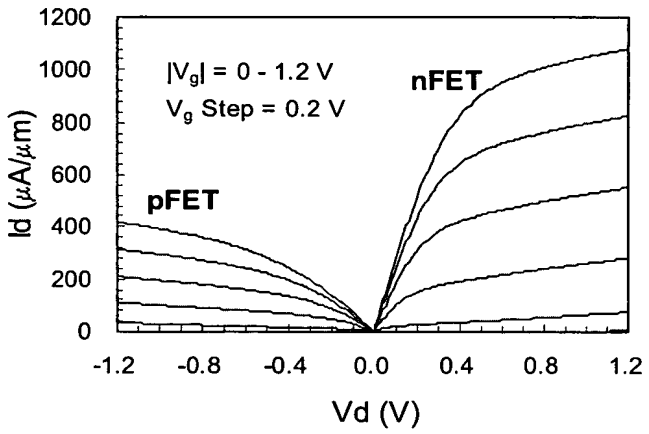


Fig. 11 Id-Vd characteristics of 55nm nFET and pFET. The drain currents at Vcc=1.0V are 800μA/um for nFET and 300μA/μm for pFET at Ioff=20nA/μm.